CLAIMS

What is claimed is:

1. An integrated circuit device comprising:

a first conductive layer including at least one protrusion;

an insulative layer overlying said first conductive layer and exposing at least part of said at least one protrusion; and

a programmable resistive material in direct contact with said at least one protrusion of said first conductive layer.

2. The integrated circuit device of claim 1, wherein said programmable resistive material is formulated to be reversibly cycled between at least two different resistive states.

3. The integrated circuit device of claim 1, wherein said exposed part of said at least one protrusion comprises a smaller cross-sectional area than a remaining part of said at least one protrusion of said at least one conductive layer.

4. The integrated circuit device of claim 1, wherein said programmable resistive material comprises a chalcogenide material.

5. The integrated circuit device of claim 4, wherein said chalcogenide material is selected from a group consisting of tellurium (Te), germanium (Ge), antimony (Sb), and combinations thereof.

6. The integrated circuit device of claim 4, wherein said chalcogenide material includes tellurium (Te), germanium (Ge), and antimony (Sb) in a ratio of $Te_aGe_bSb_{100-(a+b)}$, where a, b, and 100-(a+b) are in atomic percentages which total 100% of the constituent elements and $a \leq 70$ and $15 \leq b \leq 50$.

7. The integrated circuit device of claim 6, wherein $40 \le a \le 60$ and $17 \le b \le 44$.

8. The integrated circuit device of claim 1, further comprising a second conductive layer above said programmable resistive material.

9. The integrated circuit device of claim 8, wherein said second conductive layer comprises titanium nitride or carbon.

10. The integrated circuit device of claim 8, further comprising a conductive barrier layer between said programmable resistive material and said second conductive layer.

11. The integrated circuit device of claim 1, further comprising a second conductive layer in direct contact with said programmable resistive material.

12. The integrated circuit device of claim 1, further comprising a second conductive layer above said programmable resistive material and an interlayer dielectric over said second conductive layer, said interlayer dielectric including an aperture that exposes at least a portion of an upper surface of said second conductive layer.

13. The integrated circuit device of claim 12, further comprising a conductive grid interconnect within said aperture.

14. The integrated circuit device of claim 13, wherein said conductive grid interconnect is selected from the group consisting of titanium, titanium nitride and aluminum.

15. The integrated circuit device of claim 1, wherein a portion of said at least one protrusion comprises a frustoconical tip.

16. The integrated circuit device of claim 15, wherein said frustoconical tip has a frustum lateral dimension of at least 0.1 μm.

17. The integrated circuit device of claim 15, wherein said frustoconical tip has a frustum lateral dimension of about 0.4μm.

18. The integrated circuit device of claim 15, wherein said frustoconical tip has a height of approximately 2000 Å.

19. The integrated circuit device of claim 1, further comprising an opening through said insulative layer such said at least part of said first conductive layer is exposed.

20. The integrated circuit device of claim 19, wherein said programmable resistive material is at least within said opening.

21. An integrated circuit device comprising,

a first electrode having a first portion and a second portion, a width of the first electrode narrowing substantially and continuously in a direction extending from the second portion toward said first portion of the first electrode;

a layer of programmable resistive material in contact with said first portion of said first electrode; and

a second electrode coupled to the layer of programmable resistive material.

22. The integrated circuit device of claim 21, wherein said programmable resistive material is formulated to be reversibly cycled between at least two different resistive states.

23. The integrated circuit device of claim 21, wherein said programmable resistive material comprises a chalcogenide material.

24. The integrated circuit device of claim 23, wherein said chalcogenide material is selected from a group consisting of tellurium (Te), germanium (Ge), antimony (Sb), and combinations thereof.

25. The integrated circuit device of claim 23, wherein said chalcogenide material includes tellurium (Te), germanium (Ge), and antimony (Sb) in a ratio of $Te_aGe_bSb_{100-(a+b)}$, where a, b, and 100-(a+b) are in atomic percentages which total 100% of the constituent elements and $a \leq 70$ and $15 \leq b \leq 50$.

26. The integrated circuit device of claim 25, wherein $40 \leq a \leq 60$ and $17 \leq b \leq 44$.

27. The integrated circuit device of claim 21, wherein said second electrode comprises titanium nitride or carbon.

28. The integrated circuit device of claim 21, further comprising a conductive barrier layer between said programmable resistive material and said second electrode.

29. The integrated circuit device of claim 21, wherein said second electrode is in direct contact with said programmable resistive material.

30. The integrated circuit device of claim 21, further comprising an interlayer dielectric over said second electrode, said interlayer dielectric including an aperture that exposes at least a portion of an upper surface of said second electrode.

31. The integrated circuit device of claim 30, further comprising a conductive grid interconnect within said aperture.

32. The integrated circuit device of claim 31, wherein said conductive grid interconnect is selected from the group consisting of titanium, titanium nitride and aluminum.

33. The integrated circuit device of claim 21, wherein said first portion of said first electrode comprises a frustoconical tip.

34. The integrated circuit device of claim 33, wherein said frustoconical tip has a frustum lateral dimension of at least 0.1 μm.

35. The integrated circuit device of claim 34, wherein said frustoconical tip has a frustum lateral dimension of about 0.4μm.

36. The integrated circuit device of claim 33, wherein said frustoconical tip has a height of approximately 2000 Å.

37. The integrated circuit device of claim 21, further comprising an insulative layer above said first electrode.

38. The integrated circuit device of claim 37, further comprising an opening through said insulative layer such at least part of said first portion of said first electrode is exposed.

39. The integrated circuit device of claim 38, wherein said programmable resistive material is at least within said opening.

40. An integrated circuit device comprising:

a first electrode having a first portion and a second portion, a width of the first electrode narrowing substantially and continuously in a direction extending from the second portion toward said first portion of the first electrode;

a layer of programmable resistive material in a recess in insulative material overlying said first electrode such that said programmable resistive material is in contact with said first electrode; and

a second electrode coupled to the layer of programmable resistive material.

41. The integrated circuit device of claim 40, wherein said programmable resistive material is formulated to be reversibly cycled between at least two different resistive states.

42. The integrated circuit device of claim 40, wherein said programmable resistive material comprises a chalcogenide material.

43. The integrated circuit device of claim 42, wherein said chalcogenide material is selected from a group consisting of tellurium (Te), germanium (Ge), antimony (Sb), and combinations thereof.

44. The integrated circuit device of claim 43, wherein said chalcogenide material includes tellurium (Te), germanium (Ge), and antimony (Sb) in a ratio of $Te_aGe_bSb_{100-(a+b)}$, where a, b, and 100-(a+b) are in atomic percentages which total 100% of the constituent elements and $a \leq 70$ and $15 \leq b \leq 50$.

45. The integrated circuit device of claim 44, wherein $40 \leq a \leq 60$ and $17 \leq b \leq 44$.

46. The integrated circuit device of claim 40, wherein said second electrode comprises titanium nitride or carbon.

47. The integrated circuit device of claim 40, further comprising a conductive barrier layer between said programmable resistive material and said second electrode.

48. The integrated circuit device of claim 40, wherein said second electrode is in direct contact with said programmable resistive material.

49. The integrated circuit device of claim 40, further comprising an interlayer dielectric over said second electrode, said interlayer dielectric including an aperture that exposes at least a portion of an upper surface of said second electrode.

50. The integrated circuit device of claim 49, further comprising a conductive grid interconnect within said aperture.

51. The integrated circuit device of claim 50, wherein said conductive grid interconnect is selected from the group consisting of titanium, titanium nitride and aluminum.

52. The integrated circuit device of claim 40, wherein at least a part of said first portion of said first electrode comprises a frustoconical tip.

53. The integrated circuit device of claim 52, wherein said frustoconical tip has a frustum lateral dimension of at least 0.1 μm.

54. The integrated circuit device of claim 52, wherein said frustoconical tip has a frustum lateral dimension of about 0.4μm.

55. The integrated circuit device of claim 54, wherein said frustoconical tip has a height of approximately 2000 Å.

56. A semiconductor memory cell comprising:

a first conductive layer on a substrate, wherein said first conductive layer includes at least one raised portion;

a programmable resistive material in direct contact with said at least one raised portion of said first conductive layer; and

a second conductive layer above said programmable resistive material.

57. The semiconductor memory cell of claim 56, wherein said programmable resistive material comprises a chalcogenide material.

58. The semiconductor memory cell of claim 57, wherein said chalcogenide material is selected from a group consisting of tellurium (Te), germanium (Ge), antimony (Sb), and combinations thereof.

59. The semiconductor memory cell of claim 57, wherein said chalcogenide material includes tellurium (Te), germanium (Ge), and antimony (Sb) in a ratio of $Te_aGe_bSb_{100-(a+b)}$, where a, b, and 100-(a+b) are in atomic percentages which total 100% of the constituent elements and $a \leq 70$ and $15 \leq b \leq 50$.

60. The semiconductor memory cell of claim 59, wherein $40 \leq a \leq 60$ and $17 \leq b \leq 44$.

61. The semiconductor memory cell of claim 56, further comprising a conductive barrier layer between said programmable resistive material and said second conductive layer.

62. The semiconductor memory cell of claim 56, wherein said second conductive layer is in direct contact with said programmable resistive material.

63. The semiconductor memory cell of claim 56, further comprising an interlayer dielectric over said second conductive layer, said interlayer dielectric including an aperture that exposes at least a portion of an upper surface of said second conductive layer.

64. The semiconductor memory cell of claim 63, further comprising a conductive grid interconnect within said aperture.

65. The semiconductor memory cell of claim 64, wherein said conductive grid interconnect is selected from the group consisting of titanium, titanium nitride and aluminum.

66. The semiconductor memory cell of claim 56, wherein a portion of said at least one raised portion comprises a frustoconical tip.

67. The semiconductor memory cell of claim 66, wherein said frustoconical tip has a frustum lateral dimension of at least 0.1 μm.

68. The semiconductor memory cell of claim 66, wherein said frustoconical tip has a frustum lateral dimension of about 0.4μm.

69. The semiconductor memory cell of claim 66, wherein said frustoconical tip has a height of approximately 2000 Å.

70. The semiconductor memory cell of claim 56, wherein said second conductive layer comprises titanium nitride or carbon.

71. The semiconductor memory cell of claim 56, further comprising an insulative material over said first conductive layer and having an opening therethrough such that at least a portion of said first conductive layer is exposed.

72. The semiconductor memory cell of claim 71, wherein said programmable resistive material is at least within said opening.